In the Claims

Please replace all prior versions of claims in the application with the following list of claims:

1. (Currently amended) A method for forming in monolithic form a DRAM-type memory, including the steps of:

forming, on a single-crystal semiconductor substrate, parallel strips including a lower insulating layer, a strongly-conductive layer, a single-crystal semiconductor layer, and an upper insulating layer;

forming, perpendicularly to the parallel strips, in the upper insulating layer and in at least a portion of the single-crystal semiconductor layer, first and second parallel trenches, each of the first and second parallel trenches being shared by neighboring cells;

forming, in each of the first parallel trenches, a first conductive line according to a strip width;

forming, in each of the second parallel trenches, a pair of second distinct parallel conductive lines, insulated from ~~the~~ layers peripheral to the second trench;

filling the first and second parallel trenches with an insulating material;

removing the remaining portions of the upper insulating layer; and

depositing a conductive layer,

wherein the first and second parallel trenches are formed in the upper insulating layer and at least a portion of the single-crystal semiconductor layer so that the first parallel trenches have a minimum width, and the second parallel trenches have a width which is twice that of the first parallel trenches, two neighboring parallel trenches being separated by a minimum interval, each first trench being surrounded with two second parallel trenches and each second trench being surrounded with two first parallel trenches.

2. (Currently amended) The method of claim 1, wherein the forming of the parallel strips includes the steps of:

forming on a first single-crystal semiconductor substrate a single-crystal semiconductor layer resting on a first insulating layer;

forming, on the single-crystal semiconductor layer, a strongly-conductive layer, then a second insulating layer;

forming parallel trenches in the second insulating layer, the strongly-conductive layer, and the single-crystal semiconductor layer, to partially expose the first insulating layer;

turning over and gluing ~~the~~a structure thus obtained on a second substrate; and

removing the first single-crystal semiconductor substrate, whereby the first insulating layer becomes ~~the~~an upper layer of the structure thus formed and the second insulating layer becomes ~~the~~a lower layer underlying the single-crystal semiconductor layer.

3. (Currently amended) The method of claim 1, wherein the first and second parallel trenches are formed to maintain between the strongly-conductive layer and ~~the~~a bottom of each of the first and second parallel trenches a given thickness of the single-crystal semiconductor layer.

4. (Currently amended) The method of claim 1, wherein the first and second parallel trenches are formed to partially expose the strongly-conductive layer.

5. (Currently amended) The method of claim 1, including simultaneously forming the first conductive lines at ~~the~~a bottom of each first trench and the pairs of second parallel conductive lines at ~~the~~a bottom of the second parallel trenches.

6. (Currently amended) The method of claim 5, wherein the simultaneous forming of the first conductive lines and of the pairs of second parallel conductive lines at the bottom of the first and second parallel trenches includes the steps of:

depositing at the bottom and on ~~the~~ walls of the first and second parallel trenches an insulating layer;

conformally depositing a conductive material to at least fill the first trench; and

removing the conductive material from ~~the~~a surface of the first insulating layer.

7. (Currently amended) The method of claim 5, wherein the first conductive lines formed at the bottom of the first parallel trenches are not insulated from ~~the peripheral~~

~~semiconductor and/or conductor~~ layers peripheral to the first parallel trenches.

8. (Currently amended) The method of claim 7, including the steps of:

conformally depositing an insulating material at the bottom and on ~~the~~ walls of the first and second parallel trenches;

conformally depositing a first sub-layer of a conductive material;

performing a directional bombarding so that the conductive material is only bombarded on its sides in the second parallel trenches;

removing by selective etching ~~the sole~~ non-bombarded portions of the conductive material in the first parallel trenches;

removing ~~the~~ portions thus exposed of the insulating material previously deposited at the bottom of the first and second parallel trenches;

depositing a second sub-layer of the conductive material to at least fill the first parallel trenches; and

removing the conductive material from ~~the~~a surface of the first insulating layer.

9. (Currently amended) The method of claim 1, including, after the step of deposition of a conductive layer, the steps of:

level trimming, which results in the forming, between first and second neighboring parallel trenches, of independent conductive surfaces in contact with ~~the~~a surface of the single-crystal semiconductor layer;

depositing over ~~the~~an entire structure thus formed a thin dielectric with a high permittivity; and

depositing over the entire structure a conductive layer.

10-13. (Canceled)

14. (Currently amended) A method for fabricating a monolithic DRAM-type memory, comprising:

forming, on a single crystal semiconductor substrate, parallel strips each including a lower insulating layer, a strongly conductive layer, a single crystal single-crystal semiconductor

layer, and an upper insulating layer;

forming, perpendicular to the parallel strips, in the upper insulating layer and at least a portion of the single-crystal semiconductor layer, first and second parallel trenches, each of the first and second parallel trenches being shared by neighboring cells;

forming, in each of the first parallel trenches, a first conductive line;

forming, in each of the second parallel trenches, a pair of second conductive lines, insulated from layers adjacent to the second trench;

filling the first and second parallel trenches with an insulating material;

removing remaining portions of the upper insulating layer; and

depositing a conductive layer.

15. (Currently amended) A method as defined in claim 14, wherein the first and second parallel trenches are formed so as to maintain a given thickness of the single-crystal semiconductor layer between the strongly conductive layer and ~~the~~a bottom of each of the first and second parallel trenches.

16. (Currently amended) A method as defined in claim 14, wherein the first and second parallel trenches are formed so as to partially expose the strongly conductive layer.

17. (Currently amended) A method as defined in claim ~~1~~14, including simultaneously forming the first conductive lines in each first trench and the pairs of second conductive lines in the second parallel trenches.

18. (Currently amended) A method as defined in claim 17, wherein simultaneously forming the first conductive lines and the pairs of second conductive lines includes:

depositing an insulating layer on ~~the~~a bottom and on ~~the~~ walls of the first and second parallel trenches;

conformally depositing a conductive material to at least fill the first trench; and

removing the conductive material from ~~the~~a surface of the first insulating layer.

19. (Currently amended) A method as defined in claim 14, including, after depositing

a conductive layer, the steps of:

level trimming the structure to produce independent conductive surfaces between first and second neighboring parallel trenches;

depositing over ~~the~~an entire structure thus formed a thin dielectric with a high permittivity; and

depositing over the entire structure a further conductive layer.